IN THE UNITED STATES PATENT AND TRADEMARK OFFICE.

Applicants: Thomas, et al. Docket No.: INF 2003 P 54322 US

Serial No.: 10/790,907 Art Unit: 2822

Filed: March 2, 2004 Examiner: Au, Bac H.

For: Integrated Circuit with Re-Route Layer and Stacked Die Assembly

Mail Stop Issue Fee Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

SUBMISSION OF CITED REFERENCE

Dear Sir:

Per the Examiner's request in the Office Action dated July 11, 2006, Applicants submit herewith a copy of "Pad-On-Circuit (PoC) Process and Its Application," to Kim et al., which was previously filed in an Information Disclosure Statement on June 15, 2004.

Respectfully submitted,

February 19, 2008 /Ira S. Matsil/

Date Ira S. Matsil

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